Claims

1. A method comprising:

a host transmitting a first signal to a first device;

in response to the first signal, the host receiving a second signal;

the host detecting a presence of a second device, in response to receipt of the second signal if the host is of a first set of hosts; and

the host ignoring the second signal if the host is of a second set of hosts.

2. The method of claim 1, wherein the second device is a fail over switch.

3. The method of claim 1, further comprising:

after receiving the second signal, the host receiving a third signal from the first device;

the host transmitting the second signal to the first device; and

the host receiving a second signal from the first device.

4. The method of claim 1, performed during a handshake initialization sequence between the host and the first device.

5. The method of claim 3, wherein the second signal is a Serial ATA out of band (OOB) signal.

6. The method of claim 2, wherein the fail-over switch is a Serial ATA fail over switch.

7. A machine-accessible medium that provides instructions that, if executed by a machine, will cause said machine to perform operations comprising:

a host transmitting a first signal to a first device;

the host receiving a second signal from a second device;

the host identifying a presence of the second device, in response to receipt of the second signal;

the host receiving a third signal from the first device;

the host transmitting the second signal to the first device; and

the host receiving the second signal from the first device.

8. The machine-accessible medium of claim 7, wherein the operations are performed during a handshake initialization sequence between the host and the first device.

9. The machine-accessible medium of claim 7, wherein the second signal is a Serial ATA out of band (OOB) signal.

10. The machine-accessible medium of claim 7, wherein the medium is one of an internal logic of a circuit and an internal state machine of a circuit.

11. A machine-accessible medium that provides instructions that, if executed by a machine, will cause said machine to perform operations comprising:

a host transmitting a COMRESET to a device;

the host receiving a COMWAKE from a switch;

the host identifying a presence of the switch, in response to receipt of the COMWAKE;

the host receiving a COMINIT from the device;

the host transmitting the COMWAKE to the device; and

the host receiving the COMWAKE from the device.

12. The machine-accessible medium of claim 11, wherein the operations are performed during a handshake initialization sequence between the host and the device.

13. The machine-accessible medium of claim 11, wherein the medium is one of an internal logic of a circuit and an internal state machine of a circuit.

14. A system comprising:

a processor; and

a machine-accessible medium that provides instructions that, if executed by the processor, will cause the processor to perform operations comprising:

transmit a COMRESET to a device;

receive a COMWAKE from a fail over switch;

identify a presence of the fail over switch, in response to receipt of the COMWAKE;

receive a COMINIT from the device;

transmit the COMWAKE to the device; and

receive the COMWAKE from the device.

15. The system of claim 14, wherein the fail-over switch is a Serial ATA fail over switch.

16. The system of claim 14, wherein the operations are performed during a handshake initialization sequence between the system and the device.

17. The system of claim 14, wherein the medium is one of an internal logic of a circuit and an internal state machine of a circuit.

18. A system comprising:

a processor;

a network connection; and

a machine-accessible medium that provides instructions that, if executed by a machine, will cause said machine to perform operations comprising:

transmitting a first signal to a first device;

receiving a second signal;

identifying a presence of a second device, in response to receipt of the second signal;

receiving a third signal from the first device;

transmitting the second signal to the first device; and

receiving the second signal from the first device.

19. The system of claim 18, wherein the second device is a fail over switch.

20. The system of claim 18, wherein the operations are performed during a handshake initialization sequence between the system and the first device.

21. The system of claim 18, wherein the medium is one of an internal logic of a circuit and an internal state machine of a circuit.